This listing of claims replaces all prior versions, and listings of claims in the instant application:

Listing of Claims:

1-35. (Canceled)

36. (Currently amended) A stackable semiconductor package comprising:

a substrate having a first surface, an opposite second surface, and central through hole between the first and second surfaces;

a plurality of electrically conductive circuit patterns on each of the first and second surfaces of the substrate, wherein the circuit patterns of each of the first and second surfaces include a plurality of lands, the circuit patterns of the second surface also include a plurality of bond fingers, and at least some of the circuit patterns of the first surface are electrically connected through the substrate to some of the circuit patterns of the second surface;

a semiconductor chip in ~~said~~ the through hole, wherein the semiconductor chip has a first surface flush with the first surface of the substrate, and an opposite second surface including a plurality of conductive pads, the pads being oriented in a same direction as the second surface of the substrate, wherein the first surface of the semiconductor chip is exposed;

a plurality of conductive connecting means, wherein each of the conductive connecting means is electrically connected between a respective one of the pads of the second surface of the semiconductor chip and a respective one of the bond fingers of the

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circuit patterns of the second surface of the substrate;

a hardened encapsulant within ~~said~~ the through hole and covering the semiconductor chip therein, the bond fingers, the pads, and the conductive connecting means, wherein the lands of the circuit patterns of each of the first and second surfaces of the substrate are outward of a perimeter of the encapsulant; and

a plurality of electrically conductive balls each fused to a respective one of the lands of the circuit patterns of the first surface of the substrate.

37. (Previously presented) The stackable semiconductor package of claim 36, wherein the substrate further comprises a cover coat over the circuit patterns of the first and second surfaces of the substrate, wherein the respective lands and bond fingers are not covered by the cover coat.

38. (Previously presented) The stackable semiconductor package of claim 36, further comprising a plurality of second electrically conductive balls each fused to a respective one of the ball lands of the second surface of the substrate.

39. (Currently amended) A stack of semiconductor packages comprising:

a first semiconductor package and a second semiconductor package;

the first semiconductor package comprising: a substrate having a first surface, an opposite second surface, and central through hole between the first and second surfaces; a plurality of electrically conductive circuit patterns on each of the first and second surfaces of the substrate, wherein the circuit patterns of each of the first and second surfaces include a

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plurality of lands, the circuit patterns of the second surface also include a plurality of bond fingers, and at least some of the circuit patterns of the first surface are electrically connected through the substrate to some of the circuit patterns of the second surface; a semiconductor chip in ~~said~~ the through hole, wherein the semiconductor chip has a first surface flush with the first surface of the substrate, and an opposite second surface including a plurality of conductive pads, the pads being oriented in a same direction as the second surface of the substrate, wherein the first surface of the semiconductor chip is exposed; a plurality of conductive connecting means, wherein each of the conductive connecting means is electrically connected between a respective one of the pads of the second surface of the semiconductor chip and a respective one of the bond fingers of the circuit patterns of the second surface of the substrate; a hardened encapsulant within ~~said~~ the through hole and covering the semiconductor chip therein, the bond fingers, the pads, and the conductive connecting means, wherein the lands of the circuit patterns of each of the first and second surfaces of the substrate are outward of a perimeter of the encapsulant; and a plurality of electrically conductive balls each fused to a respective one of the lands of the circuit patterns of the first surface of the substrate; and

the second semiconductor package comprising a second substrate including second circuit patterns, a second semiconductor chip electrically coupled to the second circuit patterns, and second conductive balls fused the second circuit patterns, wherein the second semiconductor chip is electrically coupled to the second conductive balls through the second circuit patterns,

wherein the second semiconductor package is in a stack with the first semiconductor package, and at least some of the

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second conductive balls of the second package each superimpose and are electrically connected to respective ones of the lands of the circuit patterns of the second surface of the substrate of the first semiconductor package.

40. (Previously presented) The stack of claim 39, wherein the second substrate of the second semiconductor package includes a central second through hole, the second semiconductor chip is in the second through hole, and the second semiconductor package further comprises a hardened second encapsulant in the second through hole and covering the second semiconductor chip.

41. (Previously presented) The stack of claim 42, wherein the second substrate of the second semiconductor package includes a central second through hole, the second semiconductor chip is in the second through hole, and the second semiconductor package further comprises a hardened second encapsulant in the second through hole and covering the second semiconductor chip, wherein a surface of the second semiconductor chip is flush with a surface of the second substrate.

42. (Currently amended) A stack of semiconductor packages comprising:

first and second semiconductor packages each comprising: a substrate having a first surface, an opposite second surface, and central through hole between the first and second surfaces; a plurality of electrically conductive circuit patterns on each of the first and second surfaces of the substrate, wherein the circuit patterns of each of the first and second surfaces include a plurality of lands, the circuit patterns of the

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second surface also include a plurality of bond fingers, and at least some of the circuit patterns of the first surface are electrically connected through the substrate to some of the circuit patterns of the second surface; a semiconductor chip in ~~said~~ the through hole, wherein the semiconductor chip has a first surface flush with the first surface of the substrate, and an opposite second surface including a plurality of conductive pads, the pads being oriented in a same direction as the second surface of the substrate, wherein the first surface of the semiconductor chip is exposed; a plurality of conductive connecting means, wherein each of the conductive connecting means is electrically connected between a respective one of the pads of the second surface of the semiconductor chip and a respective one of the bond fingers of the circuit patterns of the second surface of the substrate; a hardened encapsulant within ~~said~~ the through hole and covering the semiconductor chip therein, the bond fingers, the pads, and the conductive connecting means, wherein the lands of the circuit patterns of each of the first and second surfaces of the substrate are outward of a perimeter of the encapsulant; and a plurality of electrically conductive balls each fused to a respective one of the lands of the circuit patterns of the first surface of the substrate,

wherein the second semiconductor package is in a stack with the first semiconductor package, and at least some of the conductive balls of the second package each superimpose and are electrically connected to a respective one of the lands of the circuit patterns of the second surface of the substrate of the first semiconductor package.

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